APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,128	04/15/2004	Peter A. Franaszck	YOR920040079US1	3127

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EXAMINER
BATAILLE, PIERRE MICHE

ART UNIT	PAPER NUMBER
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<table>
<tr><td rowspan="3">Office Action Summary</td><td colspan="2">Application No.</td><td colspan="2">Applicant(s)</td></tr>
<tr><td colspan="2">10/709,128</td><td colspan="2">FRANASZEK ET AL.</td></tr>
<tr><td>Examiner</td><td></td><td>Art Unit</td><td></td></tr>
<tr><td></td><td>Pierre-Michel Bataille</td><td></td><td>2186</td><td></td></tr>
</table>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 March 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-29</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-29</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   The present Office Action is taken in response to applicant's communication filed

22 March 2007 responding to Final Rejection dated January 24, 2007. Applicant's

amendment and/or arguments have been considered with the results that follow.

2.   Claim 1-29 are pending in the application under prosecution.

Response to Arguments

3.   Applicant's arguments, see remarks, filed 03 November 2006, with respect to the

rejection(s) of claim(s) 1-29 under 35 USC 102 in view of the reference by Keltcher et

al. (US 6,314,494) have been fully considered and are persuasive. Therefore, the

rejection has been withdrawn. However, upon further consideration, a new ground(s) of

rejection is made in view of the combination of US 6,314,494 (Keltcher et al) and US

6,973,547 (Nilsson eat al).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over US

6,134,494 (Keltcher et al) in view of US 6,973,547 (Nilsson et al).

With respect to claim 1, Keltcher discloses the invention as claimed, a system for

memory management, the system comprising: a tag controlled buffer in communication

with a memory device, said memory device including a plurality of pages divided into a

plurality of individually addressable lines, wherein said tag controlled buffer includes:

(Fig. 3; Column 1, lines 29-42; Col. 4, Lines 17-27); a prefetch buffer including at least

one of the individually addressable lines from the memory device (Fig. 1; Col. 3, Lines

11-32); and a tag cache in communication with the prefetch buffer, the tag cache

including at least one tag, wherein each said tag is associated with one of the pages in

the memory device, each said tag includes a pointer to at least one of the lines in the

prefetch buffer and access to the lines in the prefetch buffer is controlled by the tag

cache (Col. 6, Lines 4-25). Keltcher fails to specifically teach the tag including reference

history field including information about how the lines from the associated page have

been accessed in. the past and is utilized to determine which lines in the associated

page should be added to the prefetch buffer when the tag is added to the tag cache.

However, Nilsson teaches History cache 302 being a cache memory including a

plurality of entries each configured to store within a history field a history of memory

access messages associated with a corresponding data block; the history field of each

entry having a relatively deep history depth, the history field of each entry being

configured to store indications of a history of memory access requests associated with

the corresponding cache line (Fig. 3; Col. 5, Lines 28-52). Therefore, it would have been

obvious to one having ordinary skill in the at and having both teachings before him/her

at the time of the invention, to have included a plurality of entries each configured to

store within a history field a history of memory access messages associated with a

corresponding data block, as taught by Nilsson to the buffer pre-fetching system taught

by Keltcher, because the combination would provide relatively large history depths

detecting more complex memory access signatures, thus increasing prediction

accuracy, as taught by Nilsson [Col. 5, Lines 53-55].

With respect to claim 14, Keltcher discloses the invention as claimed, a system

for memory management, the system comprising: a random access memory including

at least one line, wherein each line is associated with a page in a memory device and

space in the random access memory is allocated on per line basis; a first cache device

including a plurality of tags, wherein each tag corresponds to one of the pages in the

memory device and each tag indicates the location in the random access memory of the

at least one line associated with the page (Fig. 1 & 3; Col. 1, Lines 29-42; Col. 4, Lines

17-27; Col. 3, Lines 11-32); and a tag cache in communication with the prefetch buffer,

the tag cache including at least one tag, wherein each said tag is associated with one of

the pages in the memory device, each said tag includes a pointer to at least one of the

lines in the prefetch buffer and access to the lines in the prefetch buffer is controlled by

the tag cache (Col. 6, Lines 4-25). Keltcher fails to specifically teach the tag including

reference history field including information about how the lines from the associated

page have been accessed in the past and is utilized to determine which lines in the

associated page should be added to the prefetch buffer when the tag is added to the tag

cache. However, Nilsson teaches History cache 302 being a cache memory including a

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corresponding data block, as taught by Nilsson to the buffer pre-fetching system taught

by Keltcher, because the combination would provide relatively large history depths

detecting more complex memory access signatures, thus increasing prediction

accuracy, as taught by Nilsson [Col. 5, Lines 53-55].

With respect to claims 2-20, 12-13, and 15-23, Keltcher teaches retrieving the

line corresponding to the fault line identifier from a memory device (data retrieved from

the main memory by the controller for execution to be cached in data cache); retrieving

the line corresponding to the fault identifier from the prefetch buffer via a cache line; all

of the lines in the prefetch buffer corresponding to one of the tags in the tag cache are

deleted in response to the tag being deleted from the tag cache; the system

implementing a replacement algorithm for the tags in the tag cache and for the lines in

the prefetch buffer, wherein upon insertion of a new tag into the tag cache, a sufficient

number of the tags are removed to make space for the new tag and for the prefetch

lines associated with the new tag [Col. 4, Lines 17-27; Col. 3, Lines 11-32].

6.   Claims 11, and 24-29 are rejected under 35 U.S.C. 103(a) as being unpatentable

over US 6,134,494 (Keltcher et al) in view of US 6,973,547 (Nilsson et al), as applied to

claim 1 above, and further in view of US 5,544,342 (Dean).

With respect to claim 11, Keltcher teaches a system for memory management,

the system comprising: a tag controlled (Fig. 3; Column 1, lines 29-42; Col. 4, Lines 17-

27); a prefetch buffer including at least one of the individually addressable lines from the

memory device (Fig. 1; Col. 3, Lines 11-32); and a tag cache including at least one tag,

wherein each said tag is associated with one of the pages in the memory device (Col. 6,

Lines 4-25 Nilsson teaches History cache 302 being a cache memory including a

plurality of entries each configured to store within a history field a history of memory

access messages associated with a corresponding data block; the history field of each

entry having a relatively deep history depth, the history field of each entry being

configured to store indications of a history of memory access requests associated with

the corresponding cache line (Fig. 3; Col. 5, Lines 28-52). But, neither Nilsson nor

Keltcher teaches specific reference to fault notification to access a second cache

device. However, Dean teaches receiving fault notification including a fault page

identifier and a fault line identifier, a fetch to the next level in the memory hierarchy in

response to a cache miss [Col. 31, Lines 57-62]. Therefore it would have been obvious

to one of ordinary skill in the art, having all three teachings before him/her at the time of

the invention to combine the Size Configurable Data Buffer for Data Cache and Prefetch

Cache Memory, as taught by Keltcher and reference history data being used to

determine which cacheable sub-units of the page should be pre-fetched to the cache,

as taught by Nilsson and Dean's system and Method For Prefetching Information in a

Processing System, because to utilize faults would have made the system more

efficient and diminished error handling problems.

With respect to claim 24, 25, and 29, Keltcher teaches a system for memory

management, the system comprising: a tag controlled (Fig. 3; Column 1, lines 29-42;

Col. 4, Lines 17-27); a prefetch buffer including at least one of the individually

addressable lines from the memory device (Fig. 1; Col. 3, Lines 11-32); and a tag cache

including at least one tag, wherein each said tag is associated with one of the pages in

the memory device (Col. 6, Lines 4-25); Nilsson teaches History cache 302 being a

cache memory including a plurality of entries each configured to store within a history

field a history of memory access messages associated with a corresponding data block;

the history field of each entry having a relatively deep history depth, the history field of

each entry being configured to store indications of a history of memory access requests

associated with the corresponding cache line (Fig. 3; Col. 5, Lines 28-52). But, neither

Nilsson nor Keltcher teaches specific reference to fault notification to access a second

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the invention to combine the Size Configurable Data Buffer for Data Cache and Prefetch

Cache Memory, as taught by Keltcher and reference history data being used to

determine which cacheable sub-units of the page should be pre-fetched to the cache,

as taught by Nilsson and Dean's system and Method For Prefetching Information in a

Processing System, because to utilize faults would have made the system more

efficient and diminished error handling problems.

With respect to claims 26-28, Dean teaches retrieving the line corresponding to

the fault line identifier from a memory device (data retrieved from the main memory by

the controller for execution to be cached in data cache); retrieving the line

corresponding to the fault identifier from the prefetch buffer via a cache line [Col. 31,
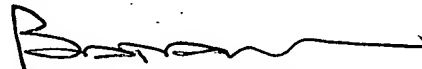
Lines 57-62].

Conclusion

1.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pierre-Michel Bataille whose telephone number is (571)

272-4178. The examiner can normally be reached on Mon, Tue-Fri (8:00A to 5:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186